Amendments to the Claims

1. (Currently Amended) A method of marking an initial defective block in a semiconductor memory device having a memory area thereof divided into a plurality of blocks and provided with an ECC function, comprising the steps of:

detecting an initial defective block; and

writing an ECC code ~~causing~~ known to cause an ECC error in a predetermined area of the initial defective block.

2. (Currently Amended) ~~The method as claimed in claim 1,~~ A method of marking an initial defective block in a semiconductor memory device having a memory area thereof divided into a plurality of blocks and provided with an ECC function, comprising the steps of:

detecting an initial defective block; and

writing an ECC code known to cause an ECC error in a predetermined area of the initial defective block,

wherein said step of writing an ECC code includes the steps of:

suspending an ECC generation function internal to said semiconductor memory device; and

writing the ECC code from an exterior of said semiconductor memory device.

3. (Currently Amended) ~~The method as claimed in claim 1~~ A method of marking an initial defective block in a semiconductor memory device having a memory

area thereof divided into a plurality of blocks and provided with an ECC function, comprising the steps of:

detecting an initial defective block; and

writing an ECC code known to cause an ECC error in a predetermined area of the initial defective block,

reading data from the initial defective block after said step of writing an ECC code;

performing an ECC check on the read data; and

rejecting said semiconductor memory device as being defective if an ECC error is not detected.

4-6. (Canceled)

7. (Previously Presented) A semiconductor memory device, comprising:

a memory area divided into a plurality of blocks;

an ECC generation circuit that generates an ECC code for data written into and for data read from an accessed block; and

an ECC suspension circuit that suspends an ECC generation function of said ECC generation circuit so as to allow the ECC code to be directly written into said memory area from an exterior of the semiconductor memory device,

wherein information about presence or absence of an ECC error is output to the exterior of the semiconductor memory device in response to a predetermined command input after a data read operation.

8. (Previously Presented) The semiconductor memory device as claimed in claim 7, wherein information about whether ECC correction is possible is output to the exterior of said semiconductor memory device.

9. (Original) The semiconductor memory device as claimed in claim 8, wherein the information about whether ECC correction is possible is output to the exterior of said semiconductor memory device in response to a predetermined command input after a data read operation.